

ELEN90053 Electronic System Design Simulation Report

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1 LTSpice Schematic

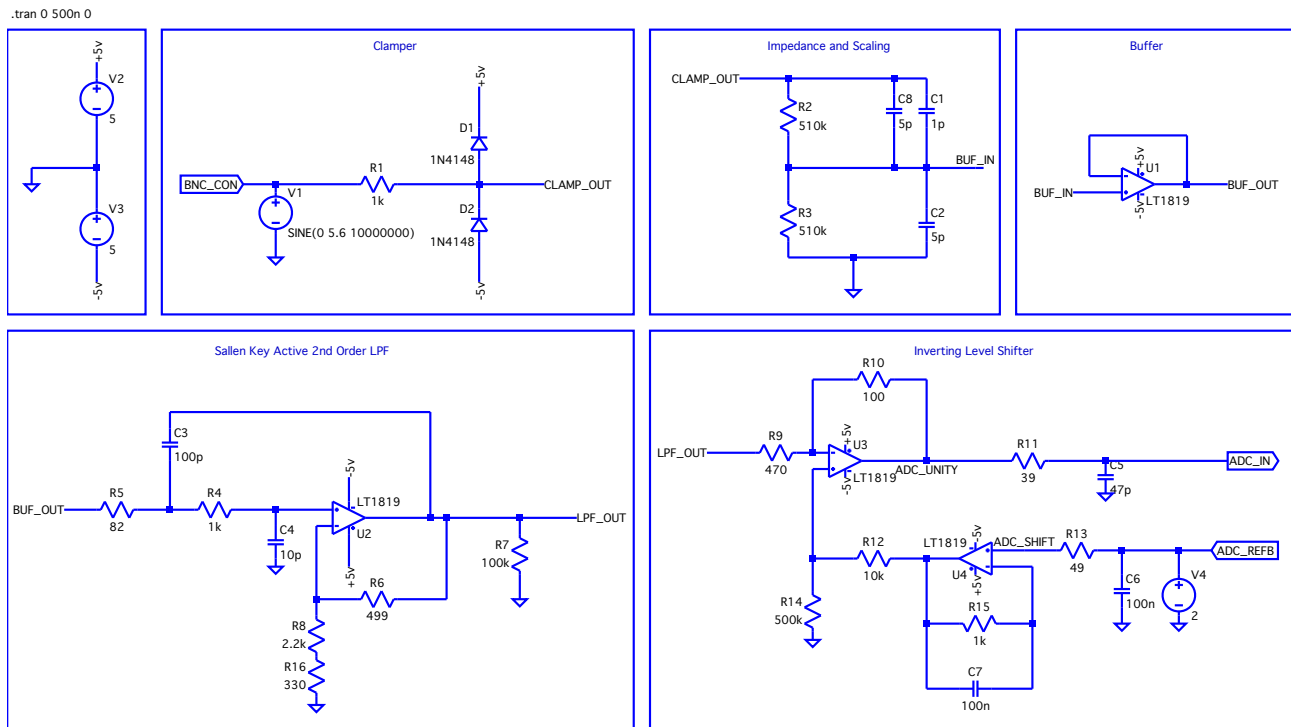


Figure 1: LTSpice Schematic

2 Frequency Response at ADC input

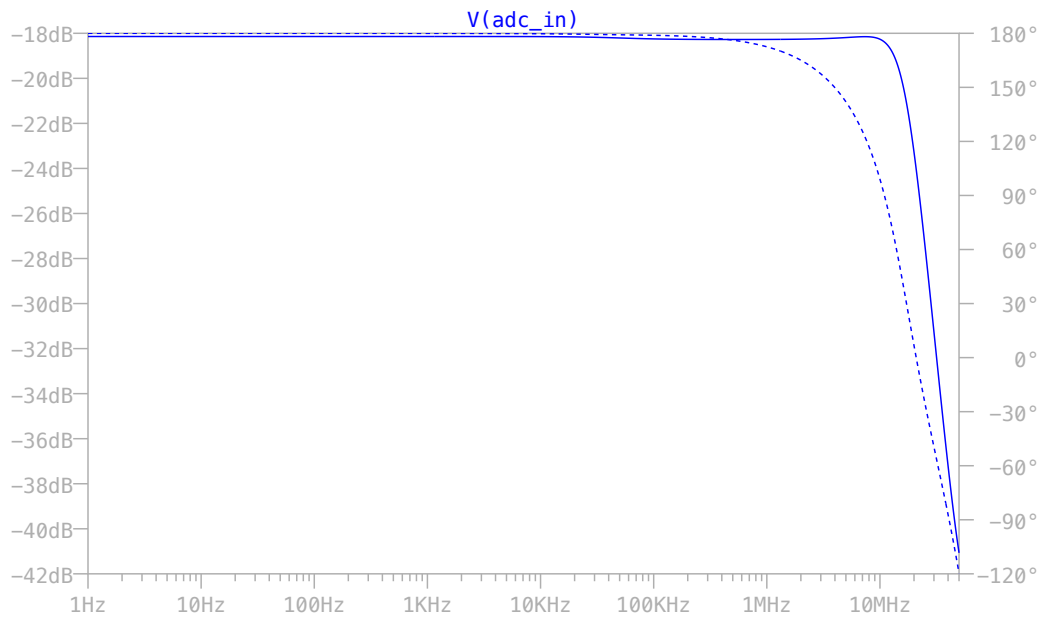


Figure 2: Frequency Response at ADC input

As can be seen from Figure 3, the cutoff frequency of ADC input is 17.233MHz, which is within the range of 17MHz to 20MHz. As an anti-aliasing filter, it can achieve a sampling rate of 40MSPS. The maximum ripple is smaller than 2dB, which is an acceptable result.

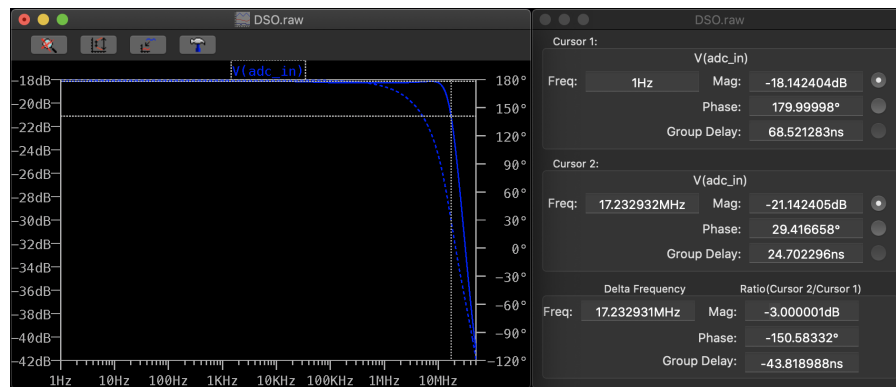


Figure 3: Magnitude Response at ADC input

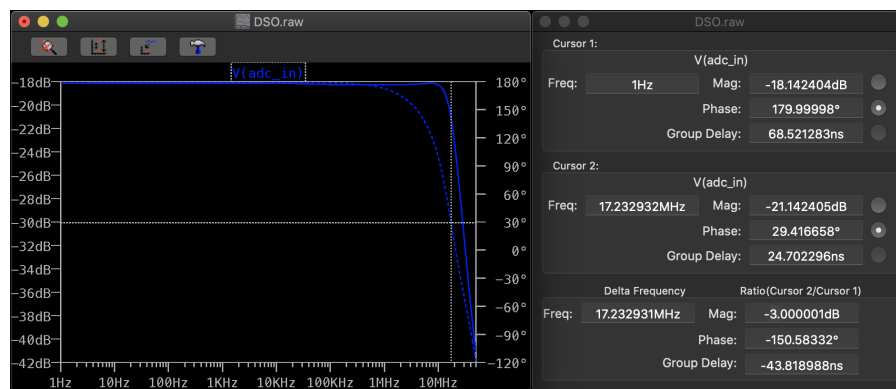


Figure 4: Phase Response at ADC input

3 Frequency Response prior to filter stage

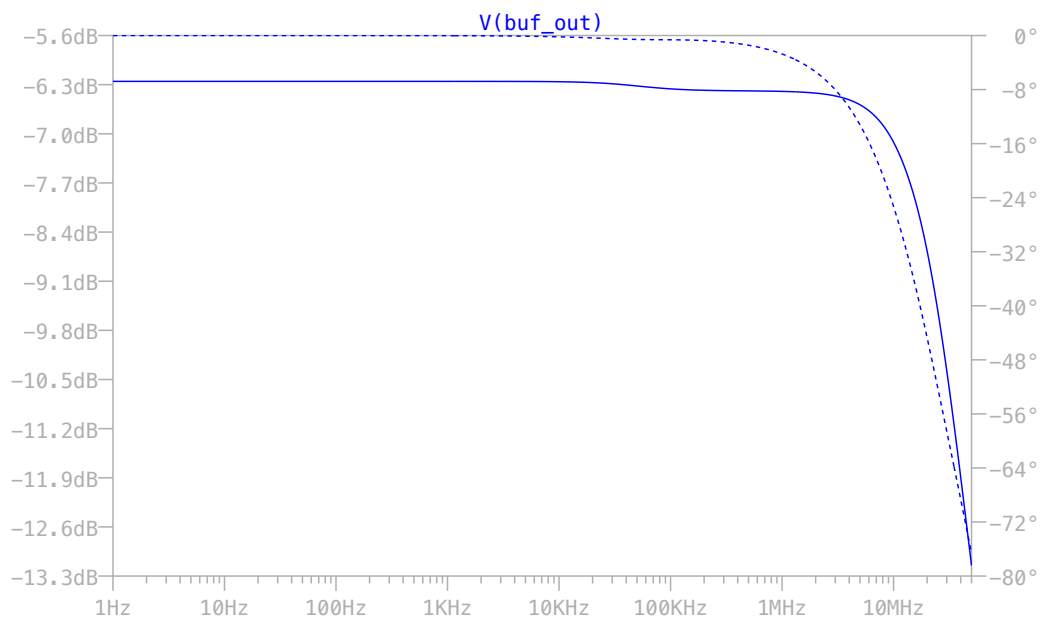


Figure 5: Frequency Response Prior to Filter Stage

4 Input Impedance at BNC Connector

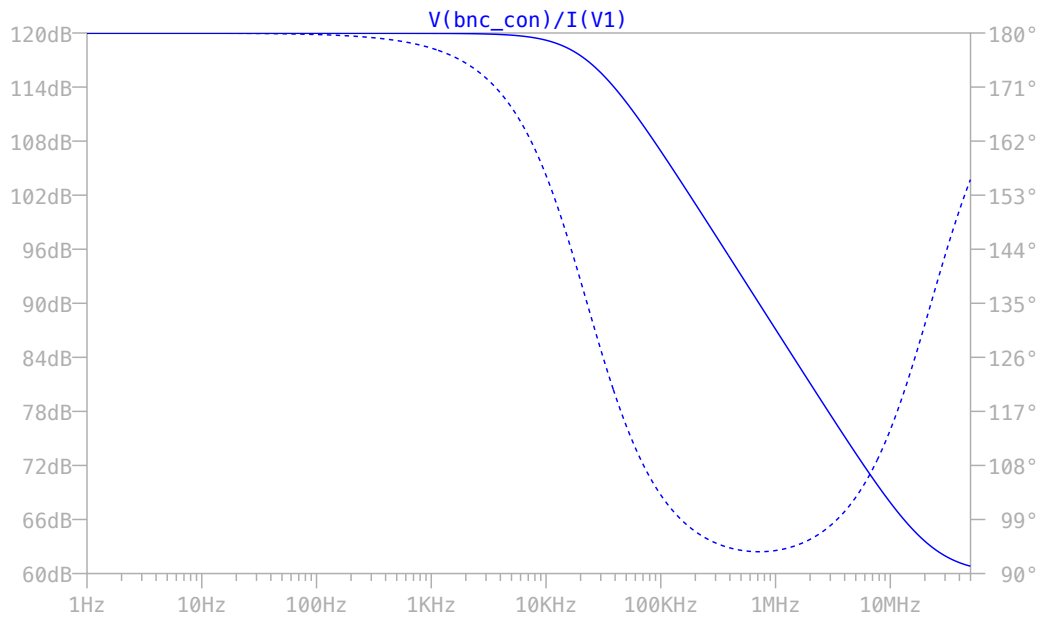


Figure 6: Input Impedance at BNC Connector

As can be seen from Figure 7, the input impedance is between $1M\Omega$ and $900k\Omega$ from DC to 10kHz. The input impedance between 10 kHz and 30 MHz is higher than 100Ω as shown in Figure 8 which also meets the requirements.

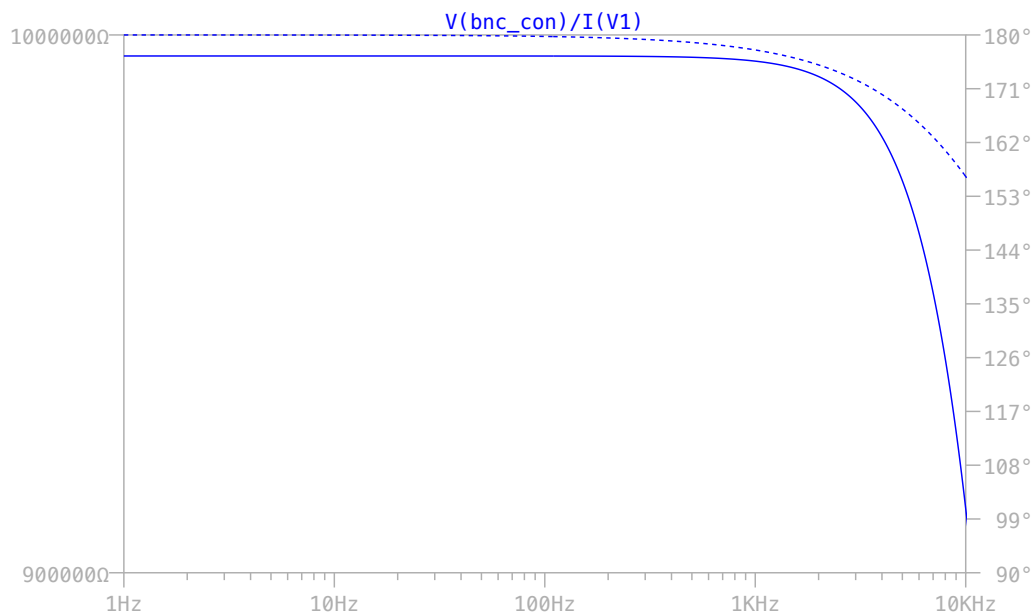


Figure 7: Input Impedance at BNC Connector (1kHz-10kHz)

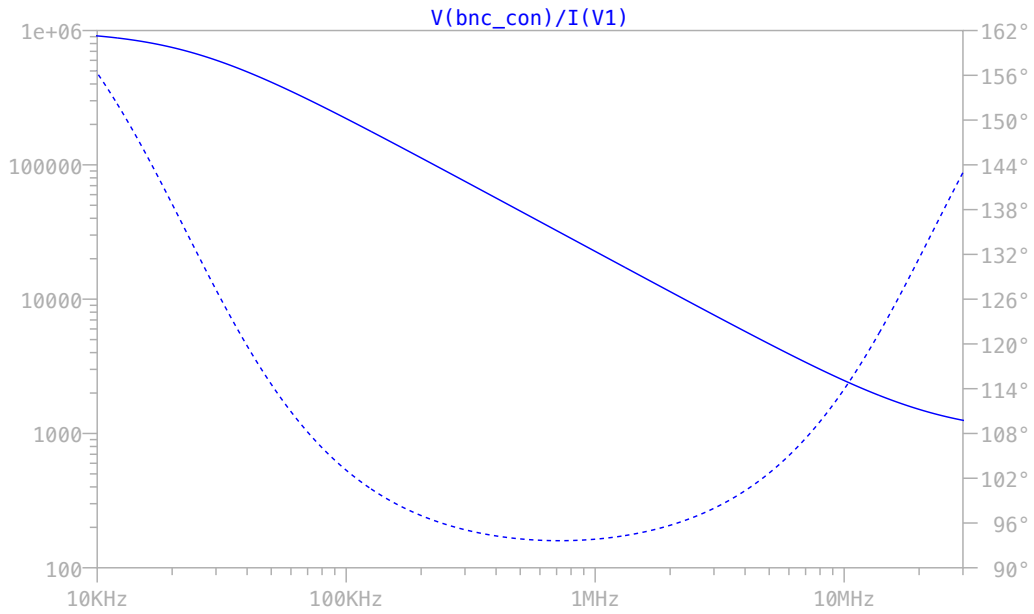


Figure 8: Input Impedance at BNC Connector (10kHz-30MHz)

5 Power Dissipation Table

Since the total current draw is limited at 150mA, the total power draw of the DSO should not exceed 0.75W with 5V supply. Also, according to the data sheet of LT1819, the maximum power dissipation should not exceed P_{DMAX} .

$$P_{DMAX} = (V^+ - V^-) \cdot (I_{SMAX}) + \frac{V^+}{2} \cdot \frac{2}{R_L}$$

$$\text{since } I_{SMAX} = 10mA$$

$$P_{DMAX} = (10V) \cdot (10mA) + (2.5V) \cdot \frac{2}{100\Omega}$$

$$P_{DMAX} = 150mW$$

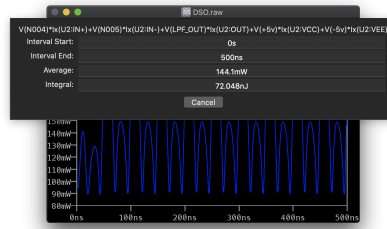
Therefore, each amplifier should not exceed maximum power dissipation of 150mW. Maximum power consumption of each amplifier can be measured as shown in Figure 9. As can be seen from Table 1, maximum power consumption of all 4 amplifiers are less than 150mW and total power consumption is less than 0.75W, which is acceptable.

Component	Net Label	Max Power Consumed(5.6V, 20MHz)
Buffer OpAmp (U1)	BUF_IN/_BUF_OUT	148.94mW
Filter OpAmp (U2)	LPF_OUT	144.1mW
First ADC OpAmp (U3)	ADC_UNITY	90.243mW
Level Shift OpAmp (U4)	ADC_SHIFT	89.98mW
	Total:	473.263mW
+5V (V2)	+5V	256.47mW
-5V (V3)	-5V	255.19mW
	Total:	511.66mW

Table 1: Power Dissipation Table



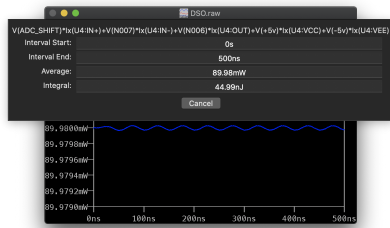
(a) Power dissipation of Buffer OpAmp



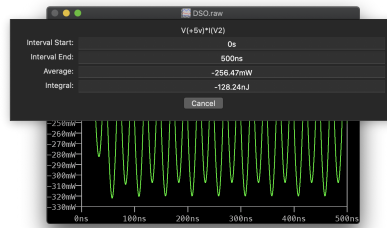
(b) Power dissipation of Filter OpAmp



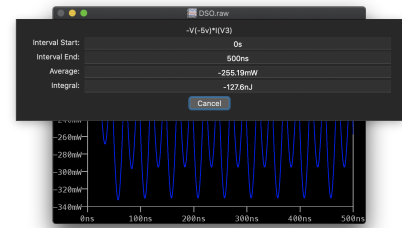
(c) Power dissipation of First ADC OpAmp



(d) Power dissipation of Level Shift OpAmp



(e) Power dissipation of +5V OpAmp



(f) Power dissipation of -5V OpAmp

Figure 9: Power Dissipation Measurement

5.1 DC Bias Table

Operating Bias Point Solution:		
V(bnc_con)	0	voltage
V(clamp_out)	0.000973748	voltage
V(+5v)	5	voltage
V(-5v)	-5	voltage
V(buf_in)	0.497585	voltage
V(buf_out)	0.497369	voltage
V(n005)	0.499237	voltage
V(n004)	0.499478	voltage
V(lpf_out)	0.59673	voltage
V(n003)	0.497529	voltage
V(p001)	0.0651178	voltage
V(n001)	1.97488	voltage
V(adc_unity)	2.26793	voltage
V(adc_in)	2.26793	voltage
V(n006)	1.99741	voltage
V(n002)	1.9759	voltage
V(adc_refb)	2	voltage
V(adc_shift)	2.00009	voltage
V(n007)	1.99921	voltage

Figure 10: DC Bias Table

As can be seen from Figure 10, the level shifter has produced a significant voltage offset, the signal from input is DC coupled. This ensures that the input voltage range of ADC meets the requirements of $2.5v \pm 1v$

6 10MHz Temporal Domain ADC Input Reading

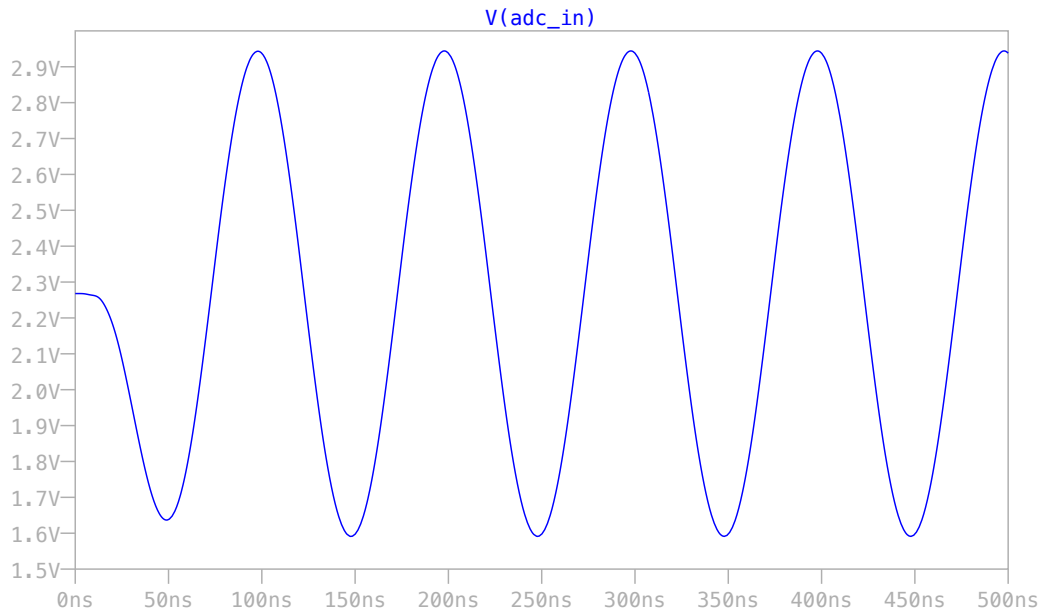


Figure 11: 10MHz Time Domain Plot at ADC Input

According to the datasheet, the maximum single end input range of ADS830 is 1.5v to 3.5v. It is clear that the waveform in Figure 11 is a 10MHz sinusoid within the maximum range of input limit, which is a acceptable result.

7 Detailed Discussion for each Block

7.1 Clamper Circuit

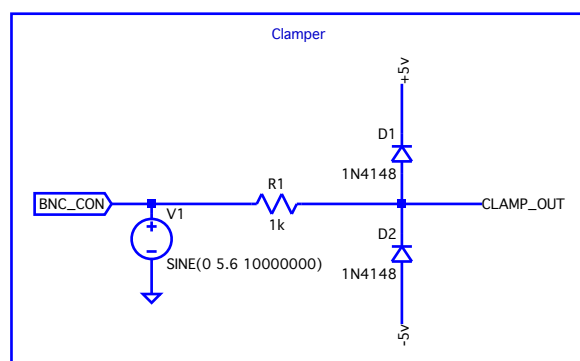


Figure 12: Clamper Circuit

As can be seen from Figure 13 and Figure 15, the clamper circuit works well with $\leq 5.6v$ input voltage. When the input voltage higher than 5.6v, the clamper circuit can protect the front end of the DSO by limiting the maximum voltage to 5.6v as shown in Figure 14.

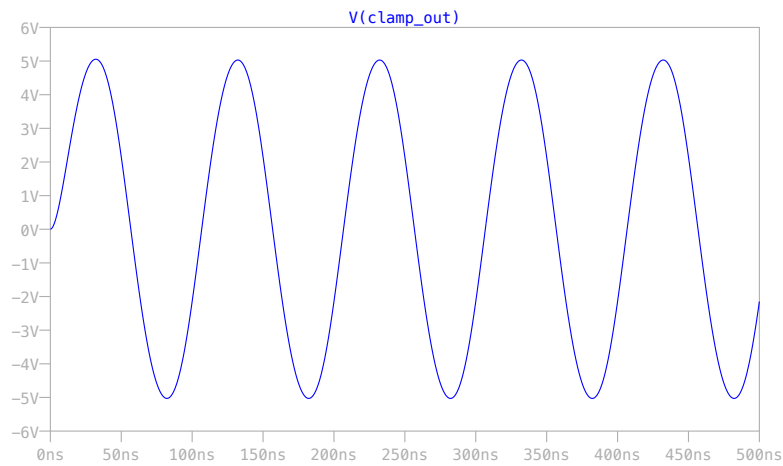


Figure 13: Clamper circuit with 5.6v input

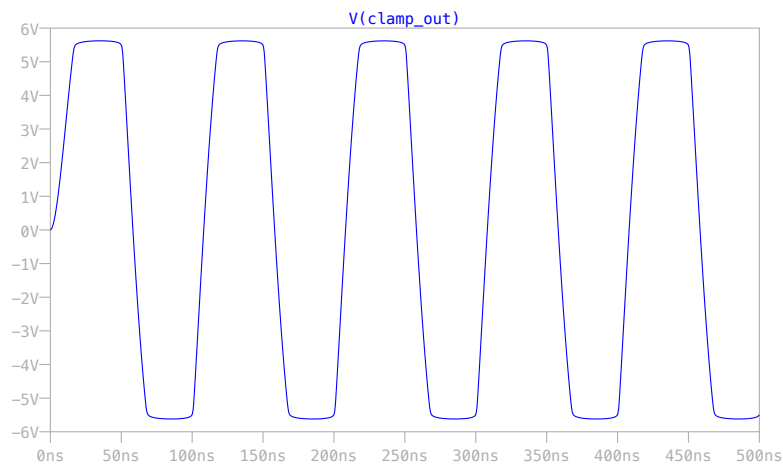


Figure 14: Clamper circuit with 10v input

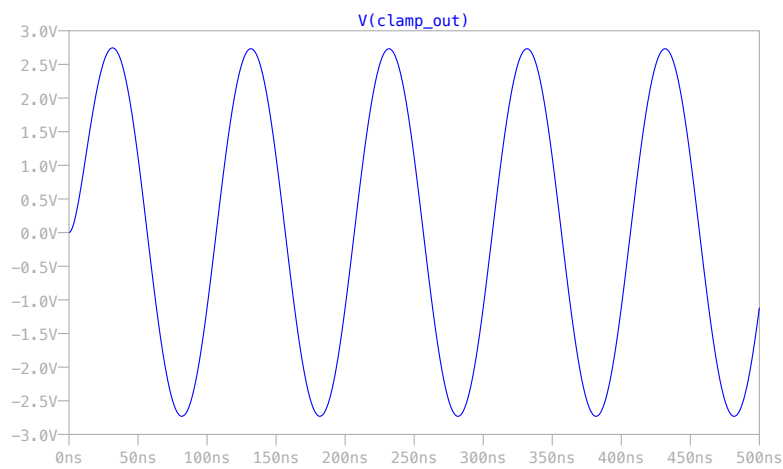


Figure 15: Clamper circuit with 3v input

Without the resistor, clamper will not work and it will output directly from the input as shown in Figure 16. However, with a large resistor, signal will be distorted as shown in Figure 17. After trial and error, I finally determined that the resistance value suitable for my circuit is 1k.

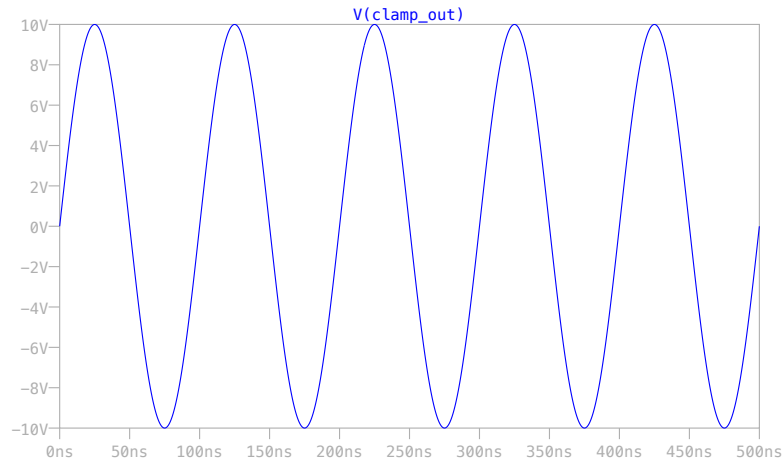


Figure 16: Clamper circuit with 10v input and no resistor

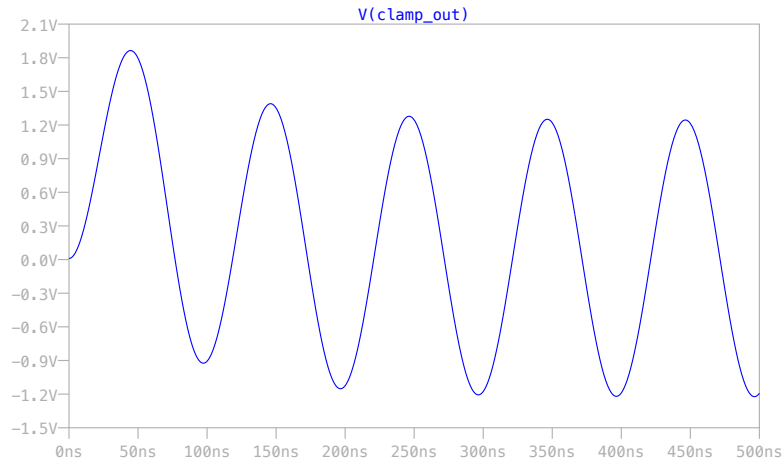


Figure 17: Clamper circuit with 10v input and 10k resistor

7.2 Impedance and Scaling Circuit

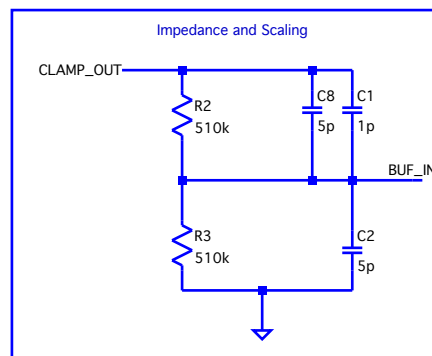


Figure 18: Impedance and scaling circuit

The impedance and scaling circuit is used to increase input impedance and scale the voltage range to the desired value. Since the input impedance requirement is $1M\Omega$, I tried some different combinations of resistors, but only one of them work with the rest of my front end circuit. Other combinations will result in some distortion in high frequency. According to the datasheet, the input voltage range of LT1819 should be within $\pm 4.2v$. Therefore, the output voltage range of BUF_IN should also be within $\pm 4.2v$. At first, I found some

combinations of single capacitor that met the voltage range requirements. However, these combinations can cause high-frequency distortion as shown in Figure 19. These distortions will increase the difficulty of filter design and may ultimately affect the results. Thus, I finally decided to use parallel capacitors to meet both the high frequency and voltage range requirements as shown in Figure 20.

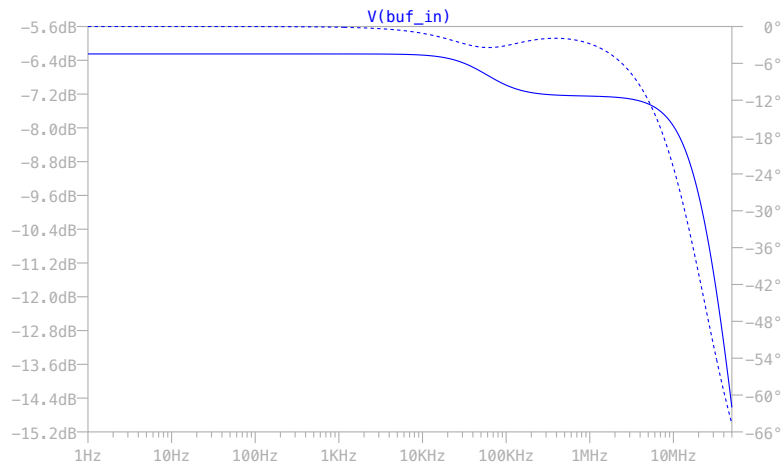


Figure 19: Example of high-frequency distortion

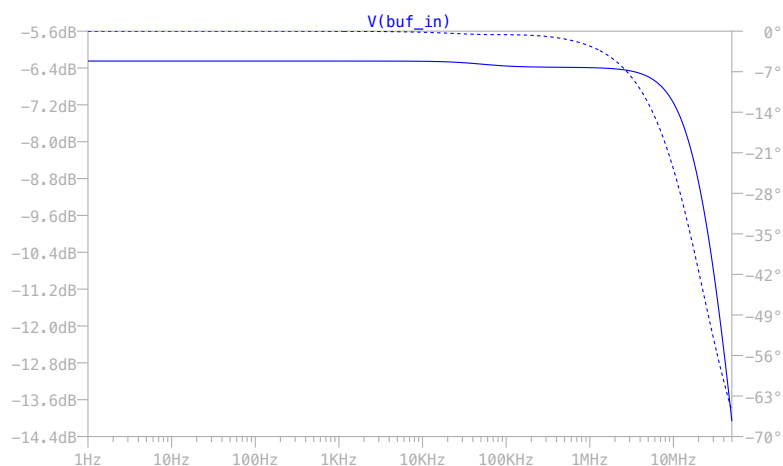


Figure 20: Output of my impedance and scaling circuit

7.3 Buffer Circuit

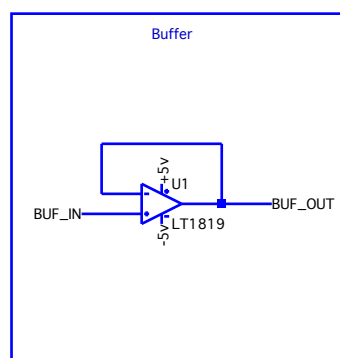


Figure 21: Buffer circuit

The buffer circuit is used to separate the circuits before and after it. It also provide an impedance transformation between two circuits and protect both circuits.

7.4 Sallen Key Active 2nd Order Low Pass Filter

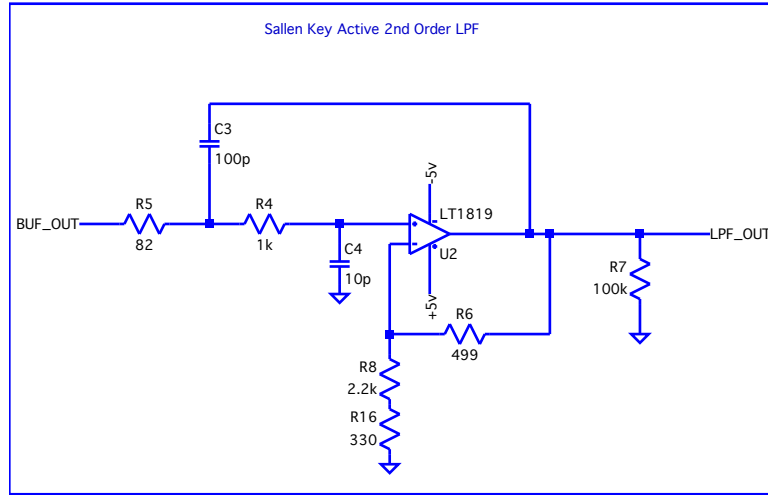


Figure 22: Sallen Key active 2nd order low pass filter

The Low-pass filter circuit is used to remove high-frequency signals and limit the signal to 20MHz as shown in Figure 23. Here I choose to use the sallent key filter to achieve the requirements. In order to design this filter, I first designed a basic 2nd order chebyshev low pass filter with ADI Filter Design Tool. Since the high frequency part of the output signal from scaling circuit is not completely smooth, I adjusted the filter to a configuration suitable for my circuit through trial and error. In addition, excessive gain and ripple will cause distortion of the output signal. In order to prevent signal distortion, I adjusted the ratio of the R6 and R8 shown in Figure 22 to made the gain within an acceptable range. Finally, the cutoff frequency is between 17 and 20, which is an acceptable result.

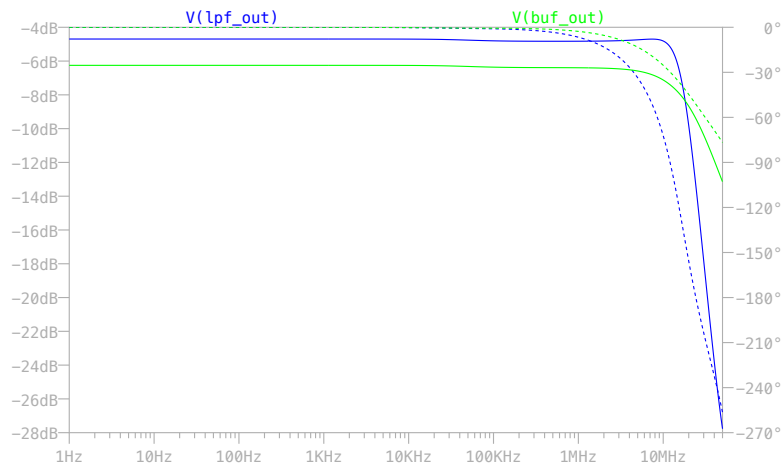


Figure 23: Input and output of low pass filter

7.5 Level Shifter and ADC

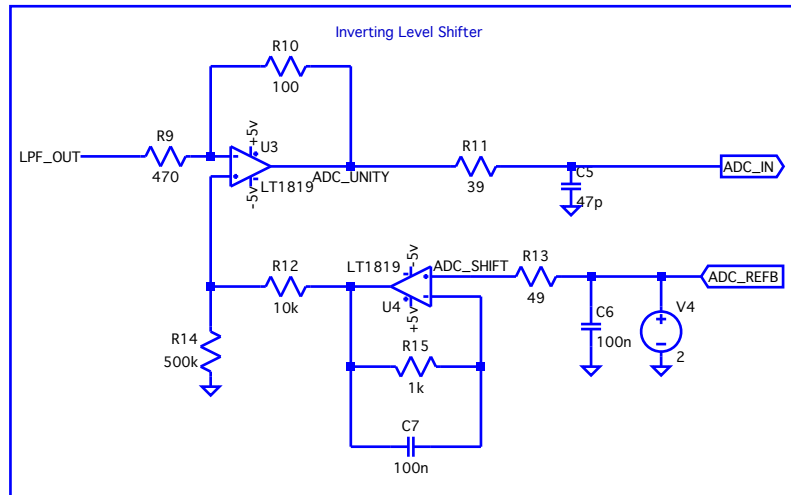


Figure 24: Level shifter circuit

The level shifter is used to convert the input signal into a signal that can be accepted by the ADC. In the previous chapter, I mentioned the ADC input signal limit, which is 1.5 to 3.5. The upper half of the circuit is used to limit the voltage range to 2v. The lower half of the circuit is used to generate an offset of 2.5v. The voltage range can be adjusted by adjusting the two resistors at the leftmost end of the upper half circuit. The voltage range decreases with the increasing of the difference between the two resistors. The voltage offset is mainly depends on the two resistors at the leftmost end of the lower half circuit, but changes in the upper half of the circuit will also affect the offset. The voltage offset increases with the increasing of the difference between the two resistors. The input and output of this module is shown in Figure 25.

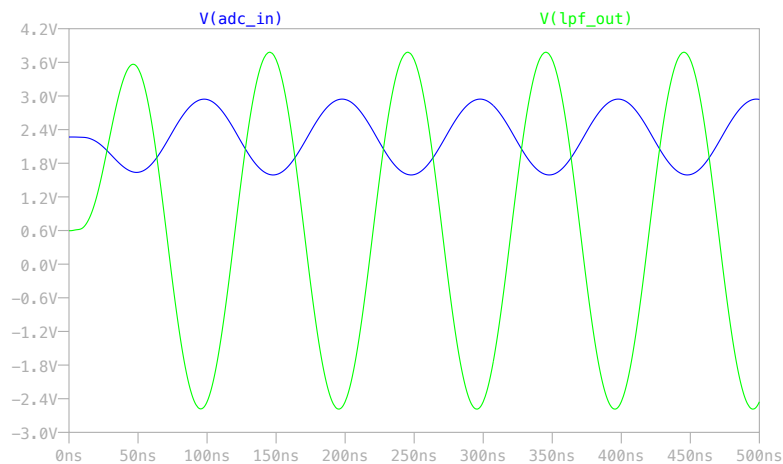


Figure 25: Level shifter circuit input and output

8 Observation of Results

With an input frequency from DC to 10kHz, the input impedance is between $1M\Omega$ and $900k\Omega$.
 With an input frequency between 10 kHz and 30 MHz, the input impedance is higher than 100Ω .
 The total input capacitance is far less than 50p.
 The input can accept a maximum input of $\pm 5.6v$ with the clamper circuit.
 The signal from input to ADC is DC coupled with a voltage offset of 2.27v.
 The anti-aliasing filter has a cutoff frequency of 17.233MHz and ripple of less than 2dB. When the input frequency is between 17MHz and 20MHz, the signal may have acceptable distortion.

9 Summary

In the design process, we used LTSpice to simulate the front-end circuit. Many unforeseen problems and difficulties appeared in the simulation process. Through a lot of trial and error on the basis of theoretical calculations, these problems were finally solved. The result of front-end design meets all input requirements and works well with maximum input voltage of 5.6v and maximum input frequency of 20MHz.